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EXAMINER	
TORRES, JUAN A	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/022,659	AZADET ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7-10,12 and 15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-10,12 and 15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Regarding claim rejections under 35 U.S.C. 112, first paragraph:

Applicant's arguments, see Amendment - After Non-Final Rejection, filed 01/25/2007, with respect to claim rejections under 35 USC § 112 first paragraph as failing to comply with the enablement requirement to claims 8, 9, 15 and 27-29 have been fully considered and are persuasive. The rejections under 35 USC § 112 first paragraph as failing to comply with the enablement requirement of claims 8, 9, 15 and 27-29 have been withdrawn.

Regarding claim rejections under 35 U.S.C. 101:

The modifications to the claims were received on 01/25/2007. These modifications are accepted by the Examiner.

In view of the amendment filed on 01/25/2007, the Examiner withdraws claim rejections under 35 USC § 101 to claims 16-22 of the previous Office action.

Regarding claims 16-19 and 22:

Applicant's arguments filed on 01/25/2007 have been fully considered but they are not persuasive.

The Applicant contends, "Raghavan discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col, 1, lines 24-36 and FIG., 1A) Thus, in Raghavan (for example, Fig,1A), the input value 1 sometimes causes a transition into the same state, and sometimes a transition into a different state. Thus, one value does not always lead to a state transition as

defined in claim 16. Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16, Compare, the Trellis of Raghavan to the MLT- trellis of the present invention. Thus, Raghaven and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two blanches leaving or entering each state, each of said at least two branches corresponding to .state transitions associated with said two binary values, wherein a first binary value substantially always causes a state transition in said trellis from a first state to a different state and a second binary value does not cause a state transition in said trellis," as required by claim 16".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Raghavan and Trans teachings are analogous art because they are from the same field of endeavor of Ethernet communications. Ethernet communications is a very specific field. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the transitions disclosed by Trans. The suggestion/motivation for doing so would have been to reduce the bandwidth of the system (column 61 lines 48-56).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

For these reasons and the reason stated en the previous Office action, the rejection of claims 16-22 are maintained.

Regarding claims 1 and 8:

Applicant's arguments filed on 01/25/2007 have been fully considered but they are not persuasive.

The Applicant contends, "MLT-3 codes are not trellis coded modulation (TCM) as described by Haratsch 1. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention. Furthermore, Haratsch 1 is addressing four dimensional TCM codes with 8 states. Thus, the branch metric computations disclosed by Haratsch 1, for example, do not make sense in the context of the present invention, For example, Equations 1 and 2 of Haratsch 1 do not make sense for MLI-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the ID branch metric to obtain 4D branch metrics for the 4D ICM code, which again does not make sense for MLT-3 codes., See also Figures 2 and 4, where one and fore dimensional branch metric units are shown".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. As indicated previously Ethernet communications is a very specific field At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3

encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "branch metric") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For these reasons and the reason stated en the previous Office action, the rejection of claims 16-22 are maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Trans (US 6377640 B2).

As per claim 16, Raghavan discloses a method for representing an MLT-3 code as a trellis, the MLT-3 code uses three signal levels to represent two binary values (figure 1A column 3 lines 37-50), the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period (figure 1A column 3 lines 37-50); generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values (figure 1A column 3 lines 37-50); and using the trellis to decode a signal encoded using the MLT-3 code (figure 1A block 96 column 4 lines 22-26). Raghavan doesn't specifically disclose that a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis. Trans discloses that a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis (column 61 lines 48-56). Raghavan and Trans teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the transitions disclosed by Trans. The suggestion/motivation for doing so would have been to reduce the bandwidth of the system (column 61 lines 48-56).

As per claim 17, Raghavan and Trans disclose claim 16. Raghavan also discloses that a first one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1 (figure 1A column 3 lines 37-50).

As per claim 18, Raghavan and Trans disclose claim 16. Raghavan also discloses that a second and third of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0 (figure 1A column 3 lines 37-50).

As per claim 19, Raghavan and Trans disclose claim 16. Raghavan also discloses that a fourth one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1 (figure 1A column 3 lines 37-50).

As per claim 22 Raghavan and Trans disclose claim 16. Raghavan also discloses an Ethernet channel (column 1 lines 11-34).

Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1).

As per claims 1 and 8, Raghavan discloses the MLT-3 encoding (column 1 lines 24-36), Raghavan doesn't disclose decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol

interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

As per claim 7 and 15, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan also discloses an Ethernet channel (column 1 lines 11-36).

As per claim 12, Raghavan and Haratsch1 disclose claim 1, Haratsch1 also a branch metric units (BMU) that calculates branch metrics based on said received signal (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); and a survivor memory unit (SMU) that stores said best surviving paths (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of

Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1). Raghavan and Trans disclose claim 16. Raghavan also discloses encoding a signal using MLT-3 code (figure 1A column 3 lines 37-50). Raghavan doesn't disclose using the trellis to perform joint equalization and decoding of an encoded signal. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan, Trans and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Trans the joint equalization and decoding disclosed by

Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Haratsch1 as applied to claims 1 and 8 above, and further in view of Haratsch ("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2).

As per claims 2 and 9, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan and Haratsch1 don't disclose a reduced complexity sequence estimation technique. Haratsch2 discloses a reduced complexity sequence estimation technique (title, abstract, introduction, and reduced complexity sequence estimation sections pages 171-174). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 10, Raghavan, Haratsch1 and Haratsch2 disclose claim 9, Haratsch2 also discloses a branch metric units (BMU) that calculates branch metrics based on said received signal (reduced complexity sequence estimation section B page

172 figure 4); an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states (reduced complexity sequence estimation section B page 172 figure 4); a survivor memory unit (SMU) that stores said best surviving paths (reduced complexity sequence estimation section B page 172 figure 4); and a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis(reduced complexity sequence estimation section B page 172 figure 4). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 23 and 27, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet

communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 24 and 28, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 26 and 29, Raghavan, Haratsch1 and Haratsch2 disclose claims 24 and 28. Haratsch2 also discloses that that number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (introduction section page 171). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are

from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 25, Raghavan, Haratsch1 and Haratsch2 disclose claim 24. Haratsch2 also discloses computing ISI estimates for the states using symbols from corresponding survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172); computing branch metrics for transitions in the trellis based on the ISI estimates (introduction, and reduced complexity sequence estimation sections pages 171-172); determining survivor paths into the states based on the branch metrics; and storing the survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch

("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2). Raghavan discloses claim 16. Raghavan doesn't disclose combining the trellis with a trellis representing a channel to obtain a super trellis. Haratsch2 also discloses combining the trellis with a trellis representing a channel to obtain a super trellis (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Trans and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the MLT-3 encoding disclosed by Raghavan and Trans the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
01-30-2007

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER